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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

Applicant : Jigish D. Trivedi  
Serial No. : 08/915,658  
Filed : August 21, 1997  
Title : LOW RESISTANCE METAL SILICIDE LOCAL INTERCONNECTS AND  
METHOD OF MAKING  
Docket : MIO 024 PA  
Examiner : G. Peralta  
Art Unit : 2814

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on November 16, 1999.

Attorney

Reg. No. 29,001

AMENDMENT

This paper is being filed in response to the Office Action mailed September 9, 1999. Reconsideration and reexamination are respectfully requested in light of the amendments and remarks below.

IN THE SPECIFICATION

At page 10, line 4, please delete "copending" and replace with --abandoned--; at line 5, please delete "(Attorney Docket No. MIO 010 PA)".

REMARKS

Applicant previously elected product claims 31-40 pursuant to a restriction requirement previously made by the Examiner. Process claims 1-30 remain in the application, but have been (presently) withdrawn from consideration by the Examiner. Thus, the cover sheet for the Office Action is incorrect in this respect by not showing the disposition of all pending claims.

Applicant's invention is directed to a local interconnect structure for use in a semiconductor device. The local interconnect is designed to electrically connect at least one of a source, drain, or gate in a field effect transistor. The local interconnect includes a composite